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IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY.(U)
MAY 78 G L VARNELL, R A WILLIAMSON DAAB07-76-C-8105
UNCLASSIFIED TI-03-78-21 NL

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Sixth Quarterly Report

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Period Covered
1 December 1977 – 1 March 1978

Contract No. DAAB07-76-C-8105

Technical Support Activity
U.S. Army Electronics Research and Development Command
Fort Monmouth, New Jersey 07703

Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265

Approved for public release; distribution unlimited.

ACKNOWLEDGMENT

This project has been accomplished as part of the U.S. Army Manufacturing and Technology Program, which has as its objective the timely establishment of manufacturing processes, techniques or equipment to ensure the efficient production of current or future defense programs.

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER

2. GOVT ACCESSION NO.

3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle)

(6) IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY.

5. TYPE OF REPORT & PERIOD COVERED

(9) Quarterly rept. no. 6,
1 Dec[redacted]977 – 1 Mar[redacted]978,

6. PERFORMING ORG. REPORT NUMBER

(14) TI-03-78-21

7. AUTHOR(s)

(10) Gilbert L. Varnell, Ronald A. Williamson, John L. Bartelt, Robert A. Owens, Jack Reynolds, ~~Roger A. Robbins~~, Claude D. Winborn

8. CONTRACT OR GRANT NUMBER(s)

(15) DAAB07-76-C-8105

9. PERFORMING ORGANIZATION NAME AND ADDRESS

Texas Instruments
P.O. Box 225012
Dallas, Texas 75265

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS

2769631

11. CONTROLLING OFFICE NAME AND ADDRESS

Technical Support Activity
U.S. Army Electronics Research and Development Command
Fort Monmouth, New Jersey

12. REPORT DATE

(11) May [redacted]78

13. NUMBER OF PAGES

19

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)

(12) 23p.

15. SECURITY CLASS. (of this report)

Unclassified

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

electron beam
e-beam resists
256-bit Bipolar RAM

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A new positive electron resist (TI-313) has been implemented for fabrication of 256-bit bipolar RAMs. This TI-313 resist has allowed plasma etching at each oxide removal step in the process. The pinhole data on this resist after oxide etch is comparable with that measured on the best standard negative photoresists. Previous attempts at fabricating the 256-bit bipolar RAMs have failed due to the high number of defects in the oxide caused by an inherent problem with PBS electron resist during wet etching. In addition, a change was made from the double-level metal 256-bit bipolar RAM (54S300) to the single-level metal 256-bit bipolar

DD FORM 1473, 1 JAN 73 EDITION OF 1 NOV 65 IS OBSOLETE

Unclassified
SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

347 650 78 11 16 001

20. ABSTRACT (Continued)

RAM (74S301A). This change was made because the TI-Houston production facility was achieving extremely low yields on the 54S200/300 and had discontinued production. These changes should allow fabrication of working devices during the next quarter.

IC FABRICATION USING ELECTRON-BEAM TECHNOLOGY

Sixth Quarterly Report

1 December 1977 – 1 March 1978

Dr. G. L. Varnell
Mr. R. A. Williamson
Dr. J. L. Bartelt
Dr. R. A. Owens
Dr. J. Reynolds
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Mr. C. D. Winborn

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SECTION I
PURPOSE

The overall objective of the program is to implement e-beam writing technology for the fabrication of microcircuits. The technical and economic impact of electron-beam direct slice printing will be demonstrated on 256-bit bipolar RAMs. The elimination of mask masters, masks, and the masking process will eliminate the most significant source of yield loss. This will permit greater circuit design complexity and flexibility which will lead to lower device costs with increased reliability. The complete implementation program is divided into three tasks. Task A, Yield Improvement Through Direct E-Beam Writing, is directed toward developing the manufacturing technology required for e-beam writing with existing equipment and existing resist processes and demonstrating the yield benefits of this technique. Task B, Cost Reduction for E-Beam Writing Through High Speed Resist Implementation, is directed toward implementing identified high speed e-beam resists in order to significantly decrease cycle time and thus reduce the IC bar cost. Task C, Cost Reduction for E-Beam Writing Through Automatic Beam Diameter Control and Automatic Handling, is directed toward utilizing EBMIII's capability of computer-controlled beam size (large and small) on high density circuit ($\leq$0.1 mil) geometries. This program also included implementation of an automated handling system for slices to reduce cycle time and thus further reduce bar cost.

SECTION II
RESULTS

A. INTRODUCTION

During this quarter, several basic decisions and changes in direction were made along with some very significant accomplishments. Lot 3 of 74S301A 256-bit bipolar RAMs was dc tested and none of the units passed all the tests. Most units passed the continuity tests but none of them passed the functional tests. The units were retested with the continuity and functional tests removed so that the device parameters could be measured. All of the tested parameters were excellent. An examination of this data, along with a vigorous visual examination of the slices, indicated the failures were caused by defects in the e-beam resist, specifically the positive resist PBS. This also correlates with pinhole data taken using PBS which indicates an abnormally high number of defects when using as an oxide etch barrier. For this reason, a TI proprietary positive electron resist (TI-313), whose development was proceeding in parallel to the contract, was phased in during this quarter. The pinhole data on this resist (after oxide etch) is comparable with that measured on the best negative photoresists such as Kodak's 747. This TI-313 resist has also allowed plasma etching at each oxide removal step in the process. In addition, a change was made from the double-level metal 256-bit bipolar RAM (54S300) to the single-level metal 256-bit bipolar RAM (74S301A). This change was made because the TI-Houston production facility was achieving extremely low yields on the 54S200/300 and had discontinued production. In addition to starting e-beam lots of the 74S301A 256-bit bipolar RAM, photomask lots were also started on the same device. This will allow a yield comparison between standard parts and e-beam delineated devices processed in the same facility. In addition, Dr. Jack Reynolds replaced Mr. Ron Williamson as chief investigator on this contract during this quarter.

B. PROCESS DEVELOPMENT

In a previous quarterly report[1], it was demonstrated that a major yield loss problem for e-beam fabrication of the 54S200/300 256-bit bipolar RAM was the high defect density generated when using PBS electron resist as an oxide etch mask. This quarter a great deal of emphasis has been placed on implementing another positive electron resist (TI-313) and its processing. TI-313 was chosen because of its speed, its compatibility with plasma processing and its low defect density. In addition, a plasma etching process compatible with TI-313 has been worked out for oxide etching at DUF and isolation.

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1. *IC Fabrication Using Electron-Beam Technology*, Contract No. DAAB07-76-C-8105, Fifth Quarterly Report (Dallas, Texas: Texas Instruments Incorporated).

A second major problem that caused difficulty with the early lots of material which were processed was the wash out of etched alignment markers during epi growth. Attempts to realign and pattern another marker set by e-beam led to significant gain and offset errors between the DUF level and the remaining levels. An alternative scheme has been developed and tested successfully which uses contact printing from two photomasks generated on EBMII to place markers on the slices before and after epi growth.

1. TI-313 Resist

Significant progress was made this quarter in implementing TI-313 positive e-beam resist and its processing to replace PBS resist for patterning the 74S301A 256-bit bipolar RAM. The details of manomer synthesis and polymerization have been well established and a high molecular weight (100K MW), narrow dispersivity, copolymer is being provided for formulation into a resist (TI-313). This resist has been evaluated for coating thickness, pinhole density, sensitivity, resolution, etch resistance, adhesion, thermal flow and thermal stability.

Xylene is used as a solvent in the formulation of TI-313 to provide the optimum combination of solubility, wettability, evaporation rate and viscosity that produces uniform defect-free coatings by spinning. A solids content in the range of 10-14% is convenient for film thicknesses in the range of 0.3-1.2 μm. A spin speed versus thickness chart for a 10% solution of TI-313 is shown in Figure 1.

Because of the etch defect problems with PBS, evaluation of TI-313 for pinhole density was one of the first tests undertaken. The procedure for visual counting of etched defects that was described in the previous quarterly report was used. For film thicknesses of 1.0 μm or greater, pinhole densities of 2/cm^2 or less were found. This compares quite favorably with standard photoresists and much better than PBS as was demonstrated last quarter.

Exposure tests on TI-313 indicate that the critical dose for proper linesize is in the range of 2 to 5 μC/cm^2 depending on thickness and development. Figure 2 shows a plot of the size of a nominally 200 μinch window as a function of dose for two different development times. Doses much in excess of 6 μC/cm^2 lead to significant amounts of crosslinked material which is not removed by development. This causes some problems in areas that are multiply scanned such as over alignment markers or areas where patterns overlap slightly because of pattern generator errors.

Patterns were developed in TI-313 by spraying for 90 seconds with a 511 mixture of 2-ethoxyethanol/2.6-dimethyl-4-heptanone followed by a 15-second rinse with 2-propanol. One of the disadvantages of TI-313 appears to be that the ratio of developing rates of unexposed to exposed resist is very low. Thus, while clearing out exposed patterns down to the substrate, 50% of

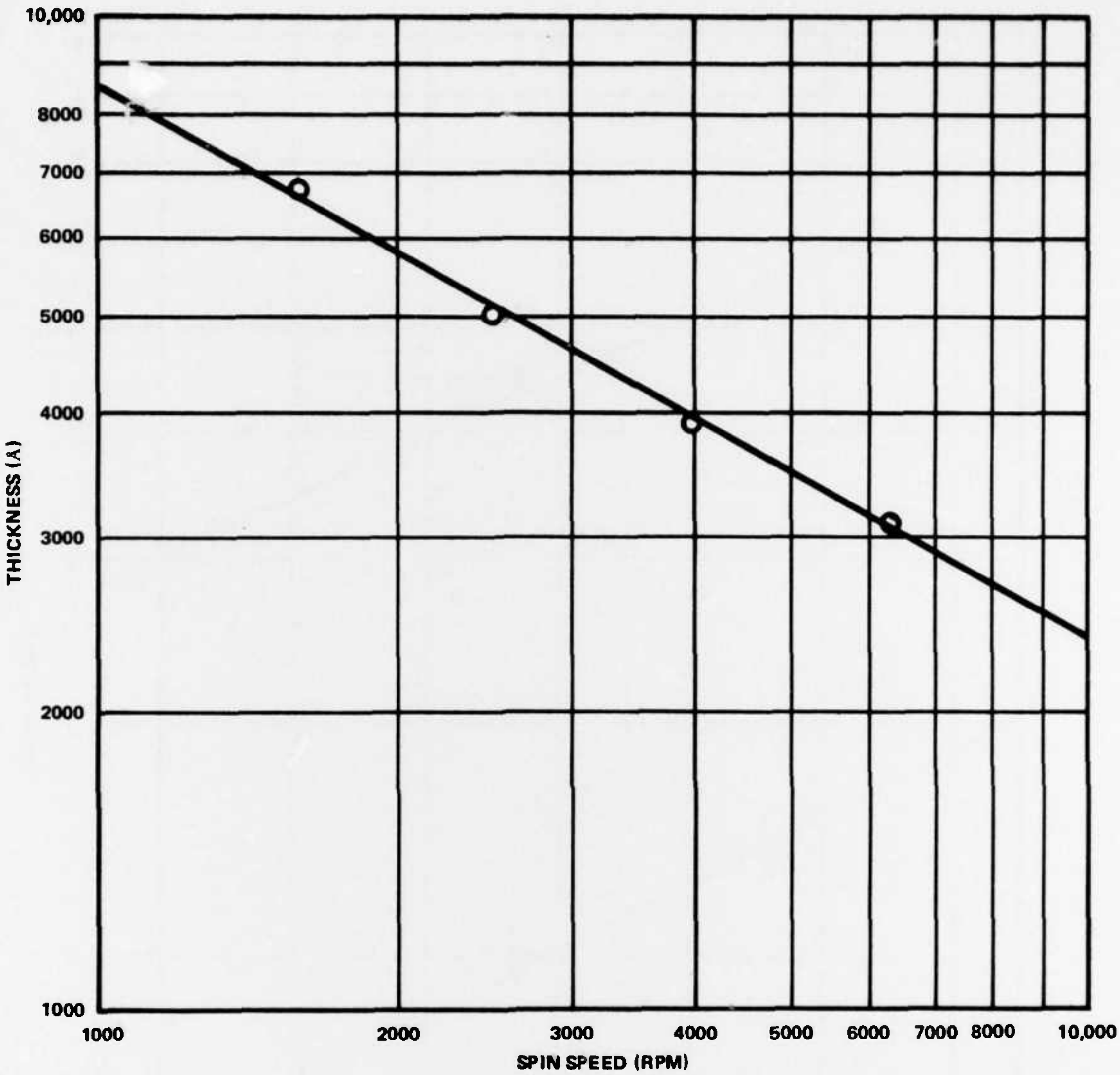


Figure 1. Spin Speed versus Thickness – TI-313 10%

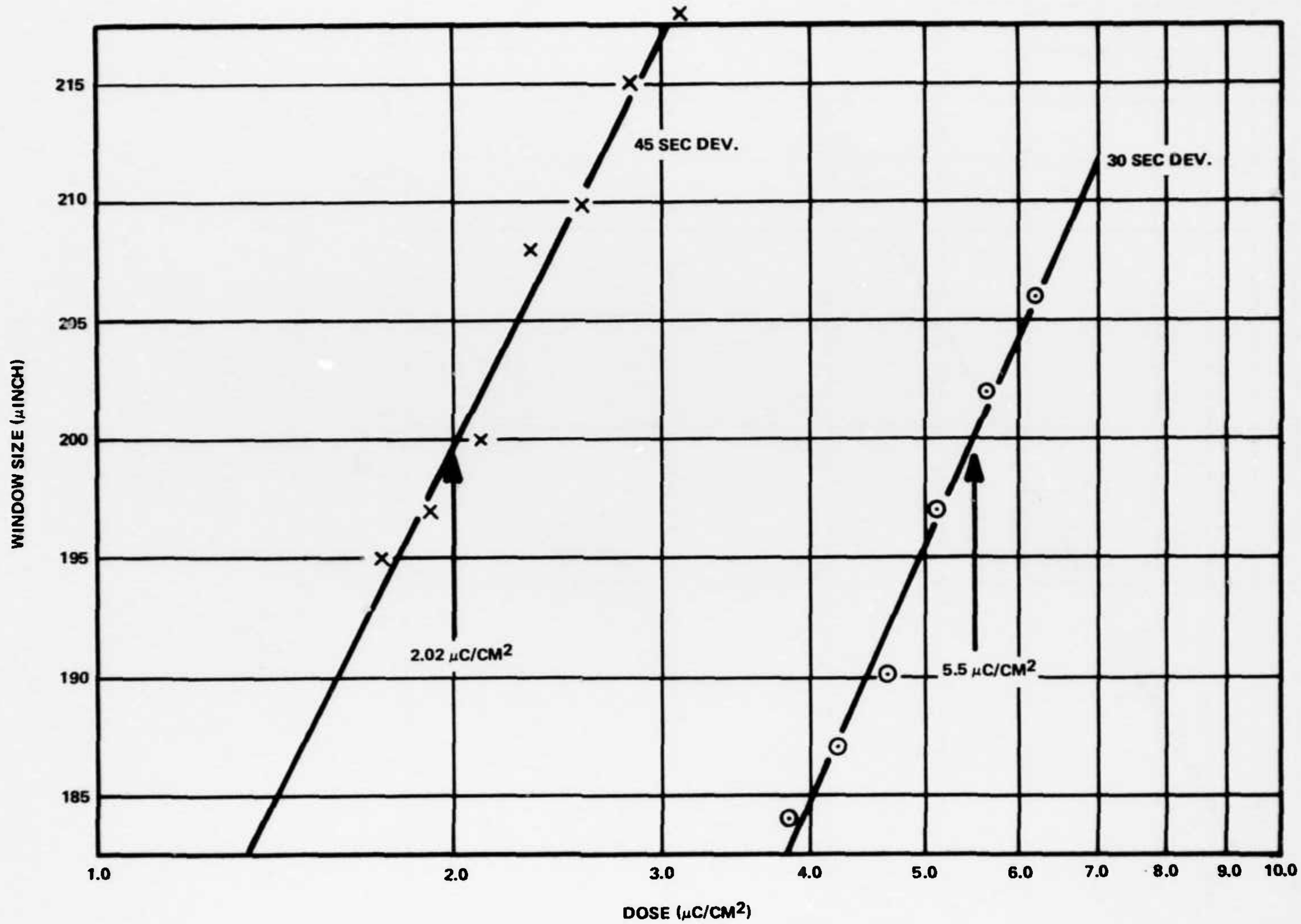


Figure 2. TI-313 Resist Developed Image Size versus Dose

the film thickness in the unexposed areas is lost. This can be a serious disadvantage in applications where step coverage, pinhole density and removal rates during etching are important.

Thermal analysis of TI-313 films have shown that the material crosslinks in the region of 170°C and begins thermal decomposition in air at about 190°C. Also patterns in the resist begin to flow at 160°C. The baking of the resist after coating and after development is done in a three-zone, belt oven at temperatures of 100-120-140°C in each zone respectively for 15 minutes.

The use of the process described above for TI-313 has been used successfully for delineating the pattern geometries required for fabrication of the 74S301.

2. Plasma Etching

Despite the useful pattern generation capability of TI-313, its adhesion to SiO^2 is poor and severe undercutting occurs when using TI-313 as a wet etch mask in buffered HF. On the other hand, TI-313 has excellent stability in plasma etching and its removal rates (50Å/min shielded, tubular type, 2000Å/min unshielded parallel plate type) are much lower than PBS or PMMA and are comparable with some negative photoresists.

A process has been developed to use TI-313 at the DUF and isolation levels to mask CF_4/O_2 etching in a shielded tubular reactor. The SiO_2 is etched down to about 1500-2000Å in the plasma and the remaining oxide is etched in buffered HF. This process yields patterns with excellent edge profiles. A brief outline of the process to be used with starting slices of 6000Å of oxide is given below:

1. Backside oxide strip
2. Coat TI-313, 2500 RPM
3. Bake, 100-120-140°C, 15 min
4. Repeat steps 2 and 3
5. Expose pattern
6. Spray develop, rinse, dry
7. Inspect and measure
8. Bake, 100-120-140°C, 15 min
9. Plasma descum, O_2, 1.5 torr, 100 W, 2 min, no tunnel

10. Plasma etch, CF_4/O_2 (4%), 1.0 torr, 300 W, 24 min, in tunnel

11. Etch to clear, buffered HF, approx. 2 min

12. Inspect

13. Plasma strip, O_2, 1.5 torr, 300 W, 15 min, no tunnel

Patterns of the DUF and isolation levels etched by this process are shown in Figures 3 and 4. Figure 5 is an SEM micrograph showing the edge profile produced by this etching.

The CF_4/O_2 plasma etching process described above cannot be used at the base, emitter or contact levels because there are at least two different thicknesses of oxide to etch at each level. When the thinnest oxide has completed etching, the silicon beneath is exposed to the very vigorous CF_4/O_2 plasma and is etched at ten times the rate of the remaining oxide. Work is currently underway to solve this problem by using a C_4F_8 plasma etch in a parallel plate reactor of the Reinberg[2] design. In some cases, conditions can be found where SiO_2 will etch at 4-5 times the rate of Si.

2. U.S. Patent, 3,757,733 issued to Texas Instruments Incorporated.

Figure 3. DUF Level (74S301A)

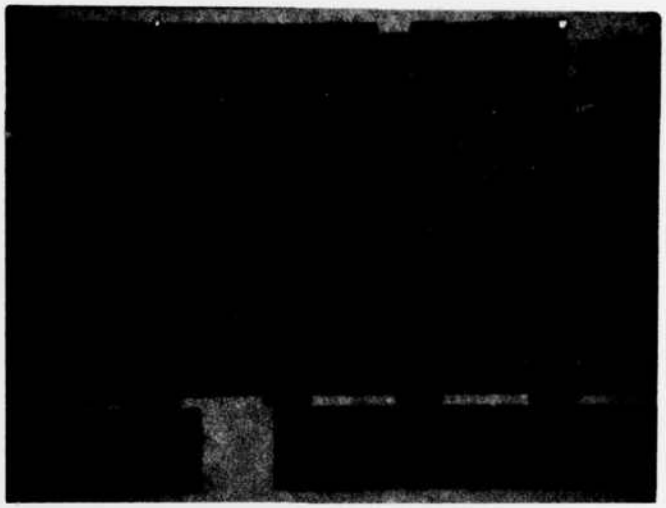
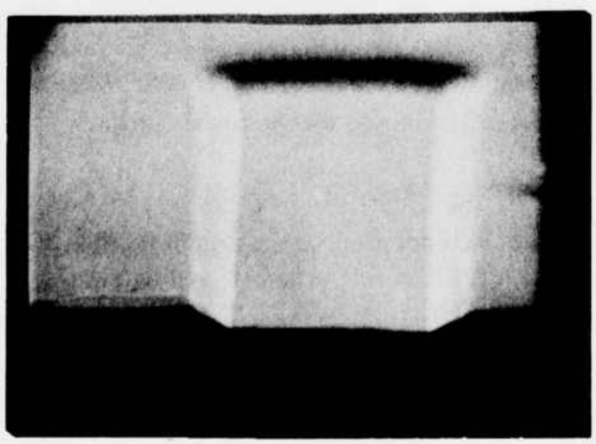


Figure 4. Isolation Level (74S301A)



SEM OF COMBINATION PLASMA ETCH/WET
ETCH PROCESS WITH TI-313

Figure 5. 256-Bit Bipolar RAM-DUF Level – 9000Å Oxide

3. Alignment Markers and Masks

Previous reports have demonstrated the wash out of alignment marks during epi growth and the difficulties encountered in trying to do automatic e-beam alignments of the post-epi levels to the pre-epi DUF level. A new method was developed which uses two photomasks fabricated on EBMIII to optically print markers which are etched into the slice. The first mask is used for pre-epi markers to which the DUF level is aligned and the second mask is optically aligned after epi to the DUF level to give markers for alignment of all subsequent levels. Results from the use of this scheme on the first lots of 74S201A to be fabricated have shown realignment accuracies of $\pm 1\ \mu m$ between the DUF isolation levels. This is more than adequate for DUF alignment since this is normally the least critical tolerance.

Besides the first two alignment mark masks which are used as described previously, a third mask has been generated which can be used to clear oxide residues which remain in the vicinity of the e-beam markers after etching. These residues are a result of e-beam resist which is crosslinked during the alignment scans and not removed by development. Modification to the alignment scan routine and modifications to the TI-313 electron resist are being investigated as alternate solutions to the problem.

C. SLICE PROCESSING

1. General Discussion

All effort on building the 54S200/S300 at the TI production facility in Houston has ceased due to extremely low yields caused by a circuit design problem. In view of this fact, the implementation of e-beam writing technology with the 250-bit bipolar RAM has been redirected to 74S201A/S301A. This single-level metal 256-bit bipolar RAM is currently being built in Houston with a sufficiently high yield to make it suitable for the e-beam program.

In order to properly evaluate the e-beam processing system for building the 74S201A/S301A, each lot of material processed will be accompanied by a lot processed by conventional contact print resist techniques. Indeed several lots of contact print lots will be processed in the SREL pilot line facility in order to establish a yield capability data point.

2. Process Description

The process to be used for building the e-beam version of the 74S201A/S301A is given in detail in Table I and Figure 6. The contact print monitor lots are processed exactly on the e-beam material except for the resist steps which will be done by conventional contact printing. The e-beam resist steps listed in Table I are discussed in detail in Section II.B.2.

Table I. Process Flow for E-beam 74S201A/74S301A

Step				
1	**Substrate**			
	Type:	P		
	Dopant:	Boron		
	Resistivity:	10-20 ohm-cm		
	Orientation:	1-1-1		
	Diameter:	3"		
2	**1st Marker Mask**			
	Piranha Clean			
	Spin Swab/Inspect			
	Bake:	30 minutes	Blue M oven	200°C
	Coat:	3.5K RPM	Waycoat III	23 cps for 7KA
	Softbake:	60 minutes	Vacuum oven	80°C
	N_2 Dry:	30 minutes plus		
	A&E:	Tower 114	8.0 seconds	
	Develop/Rinse/ Dry:	Stoddard/Butyl/N_2		
	Inspect:			
	Silicon Etch	SREL E-Beam Lab		
3	**First Oxidation**			
	Pirenha Clean			
	Spin Sweb/Inspect			
	Oxide Temp:	1300°C cycled from 850°C		
	Time:	360 minutes		
	Gas:	O_2 4 l/minutes		
	Furnace:	Silicon Tube/Boat		
	Inspect			
	Measure Oxide Thickness:	6400A		
4	**Backside Strip OR**			
	Coat:	5.0K RPM	Waycoat III	23 cps for 6400A
	Softbake:	10 minutes	IMS Oven	65°C
	A&E:	Blank Mask	8.0 seconds	
	Develop			
	Inspect			
	Hardbake:	10 minutes	IMS Oven	125°C
	Etch Backside:	7.5 minutes	Bell 2	30°C
	Rinse:	Cold DI H_2O	5 minutes	3X
	Spray Rinse/ Dry:	5/4 minutes		
	Inspect			
	Piranha Clean			
5	**DUF OR SREL E-Beam Lab**			

Table 1. Process Flow for E-beam 74S201A/74S301A (Continued)

Step				
6	**DUF Diffusion**			
	Pirenhe Cleen and edd "P" type pilots			
	Inspect			
	Deglaze:	30 seconds	10% HF	Room Tempereture
		(Will remove approximetely 170Å)		
	Spin Arsenic:	1000A } Linear Circuits		
	Bake:	2 minutes 165°C } Linear Circuits		
	Inspect			
	Deposition	Temp:	1100°C cycled from 850°C	
		Time:	50 minutes	
		Gas:	O_2N_2	O_2 150 cc/min N_2 2.85 l/min
		DUF Window:	1050A	
		Field Oxide:	7450A	
	Inspect			
	Strip Pilot:	49% HF	1 minute	
	Measure and Record			
	Resistivity Spec:	23-27 Ω/sq.		
	Steam Deglaze:	Temp:	1000°C cycled from 850°C	
		Time:	15-30-5	
		Gas:	O_2-Steam-N_2	O_2 2 l/min N_2 2 l/min
		DUF Window:	4265A	
		Field Oxide:	8000A	
	Strip Pilot and Read			
	Rs Spec:	29-35 Ω/sq.		
	Deglaze:	4.0 minutes	10% HF	Room Temperature
	Avg. Etch Rate			
	Per Minute:	DUF Window:	418A	
		Field Oxide:	450A	
	Oxide Left for			
	Drive:	DUF Window:	2500A	
		Field Oxide:	6200A	
	Drive:	Temp:	1300°C cycled from 850°C	
		Time:	300 minutes	
		Gas:	O_2 2 l/min	
	Oxide After Drive:	DUF Window:	7000A	
		Field Oxide:	8300A	
	Strip Pilot:	Read Rs and Xj Spec:	Rs 12-17 Ω/sq. Xj 35-45 HG Lines	
	Strip Slices	49% HF	3.0 minutes	
	Groove one slice to check if eny penetretion end/or damage.			
7	**Epi**			
	Pirenha Cleen			
	Spin Sweb			
	Epi:	HCl Etch:	4 HG Lines	
		Thickness:	.10 - .11 mils	
		Resistivity:	.28 - .32 Ω/cm	
		Evaluate and Record R&T		

Table I. Process Flow for E-beam 74S201A/74S301A (Continued)

Step					
8	**2nd Marker Mask**				
	Repeat Step 2, except use 2nd marker mask				
9	**2nd Oxidation**				
	Piranha Clean				
	Spin Swab/Inspect				
	Oxide:	Temp:	1000°C cycled from 850°C		
		Time:	15-70-5		
		Gas:	O_2-Steam-N_2		O_2-2 l/min
					N_2-2 l/min
	Inspect				
	Measure Oxide				
	Thickness:	5400A			
10	**Backside Strip OR**				
	Repeat Step 4				
11	**Isolation OR SREL E-Beam Lab**				
12	**3rd Marker Mask OR**				
	Piranha Clean				
	Inspect				
	Bake:	30 minutes	Blue M oven	200°C	
	Coat:	5K RPM	Waycoat III	23 cps for 6000A	
	Softbake:	10 minutes	IMS Oven	65°C	
	A&E:	Tower 114	8.0 seconds		
	Develop				
	Inspect				
	Hardbake:	10 minutes	IMS Oven	125°C	
	Etch:	To clear 2nd marker windows			
	Inspect				
	Piranha				
13	**Isolation Diffusion**				
	Inspect				
	Deposition:	Temp:	1100°C cycled from 850°C		
		Source:	BBr_3		
		Time:	25-45-5		
		Gas:	N_2O_2 - $N_2O_2N_2$ - N_2O_2		O_2-200 cc/min
					N_2 Source-30 cc/min
					N_2-7 l/min
	Steam Deglaze:	Temp:	750°C		
		Time:	10-20-5		
		Gas:	O_2-Steam-N_2		O_2-2 l/min
					N_2-2 l/min
	Deglaze:	2.0 minutes	10% HF	30°C	
	Measure Rs				
	on Pilot:	4-5 Ω/sq.			

Table I. Process Flow for E-beam 74S201A/74S301A (Continued)

Step				
13	**Isolation Diffusion (Continued)**			
	Drive:	Temp:	1100°C cycled from 850°C	
		Time:	30-10-5	
		Gas:	O_2-Steem-N_2	O_2-2 l/min N_2-2 l/min
	Inspect			
	Meesure Oxide Thickness:	3200-3400A		
	Strip Pilot end Read Rs	5-7 Ω/sq.		
	Xj Pilot:	10-11 HG Lines		
14	**Backside Strip OR**			
	Repeet Step 4			
15	**Base OR SREL E-Beam Lab**			
16	**3rd Marker Mask OR**			
	Repeat Step 12			
17	**Base Diffusion**			
	Inspect:	Add "N" Pilots		
	Pre-Heat:	Temp:	700°C	
		Source:	Boron Nitride	
		Time:	10 minutes	
		Gas:	N_2 2 l/min	
	Deposition:	Temp:	950°C	
		Source:	Boron Nitride	
		Time:	45 minutes	
		Ges:	N_2 2 l/min	
	Steam Degleze:	Temp:	750°C	
		Time:	10-20-5	
		Gas:	O_2-Steam-N_2	O_2-2 l/min N_2-2 l/min
	Deglaze:	2.0 minutes	10% HF 30°C	
	Measure Rs on Pilot:	58-66 Ω/sq.		
	Inspect			
	Drive:	Temp:	1050°C cycled from 850°C	
		Time:	30-15-75	
		Gas:	O_2-Steem-N_2	O_2-2 l/min N_2-2 l/min
	Inspect			
	Measure Oxide Thickness:	3200-3400A		
	Strip Pilot and Read Rs:	170-190 Ω/sq.		
	Xj Pilot:	4.5-5.5 HG Lines		

Table I. Process Flow for E-beam 74S201A/74S301A (Continued)

Step				
18	**Backside Strip OR**			
	Repeat Step 4			
19	**Emitter OR SREL E-Beam Lab**			
20	**3rd Marker Mask OR**			
	Repeet Step 12			
21	**Emittar Pilot Deposition**			
	Inspect			
	Deposition:	Temp:	1000°C	
		Source:	$POCl_3$	
		Time:	5-9-1-4-1	
		Gas:	N_2O_2 - $N_2O_2N_2$ - N_2O_2 - N_2O_2 + Steam	N_2O_2
				O_2-300 cc/min
				N_2 Source-300 cc/min
				N_2-2 l/min
	Measure Oxide Thickness:	2000Å		
	Strip Pilot and Read Rs:	5-7 Ω/sq.		
	Xj Pilot:	3-4 HG Lines		
22	**Backside Strip OR**			
	Repeet Step 4			
23	**Contact OR SREL E-Beam Lab**			
24	**Piranha**			
25	**Emittar Pilot Anneal/Probe**			
	Anneal:	Temp:	450°C	
		Time:	5-60-5	
		Gas:	Argon-H_2-Argon	Argon 4.5 l/min; H_2 0.5 l/min } O_2 Scales
	Probe:	NPN β_F	30-60	
26	**Emittar Lot Deposition**			
	Repeet Steps 21 thru 24			
27	**Evaporation**			
	Piranha Clean			
	Inspect			
	Pletinum Sputter:	500Å		
	inspect			
	Aque Regia:	10 minutes		
	inspect			
	Prienha Clean			

Table I. Process Flow for E-beam 74S201A/74S301A (Concluded)

Step				
27	**Evaporation (Continued)**			
	Spin Swab/Inspect			
	TiW Sputter:	1500A		
	Aluminum Evap:	Thickness:	55 microinches	
		Substrate Temp:	200°C	
	Measure Aluminum Thickness			
	Inspect			
28	**Aluminum/TiW Removal SREL E-Beam Lab**			
29	**J-100 Clean**			
30	**Sinter/Probe**			
	Sinter:	Temp:	450°C	
		Time:	60 minutes	
		Gas:	O_2N_2	O_2 50 cc/min
				N_2 2 l/min
	Probe:	NPN β_F	30-60	
31	**Nitride Deposition**			
	Spray Rinse/Spin Dry:	Cold DI H_2O		
	Inspect			
	Deposition:	Temp:	230°C	
		Thickness:	3000A	
32	**Nitride OR SREL E-Beam Lab**			
33	**Etch and Ash**			
	Etch:	8.0 minutes	100°C	
	Ash:	25 minutes		
34	**J-100 Clean**			
35	**Multi Probe: CDD Measurements Lab**			

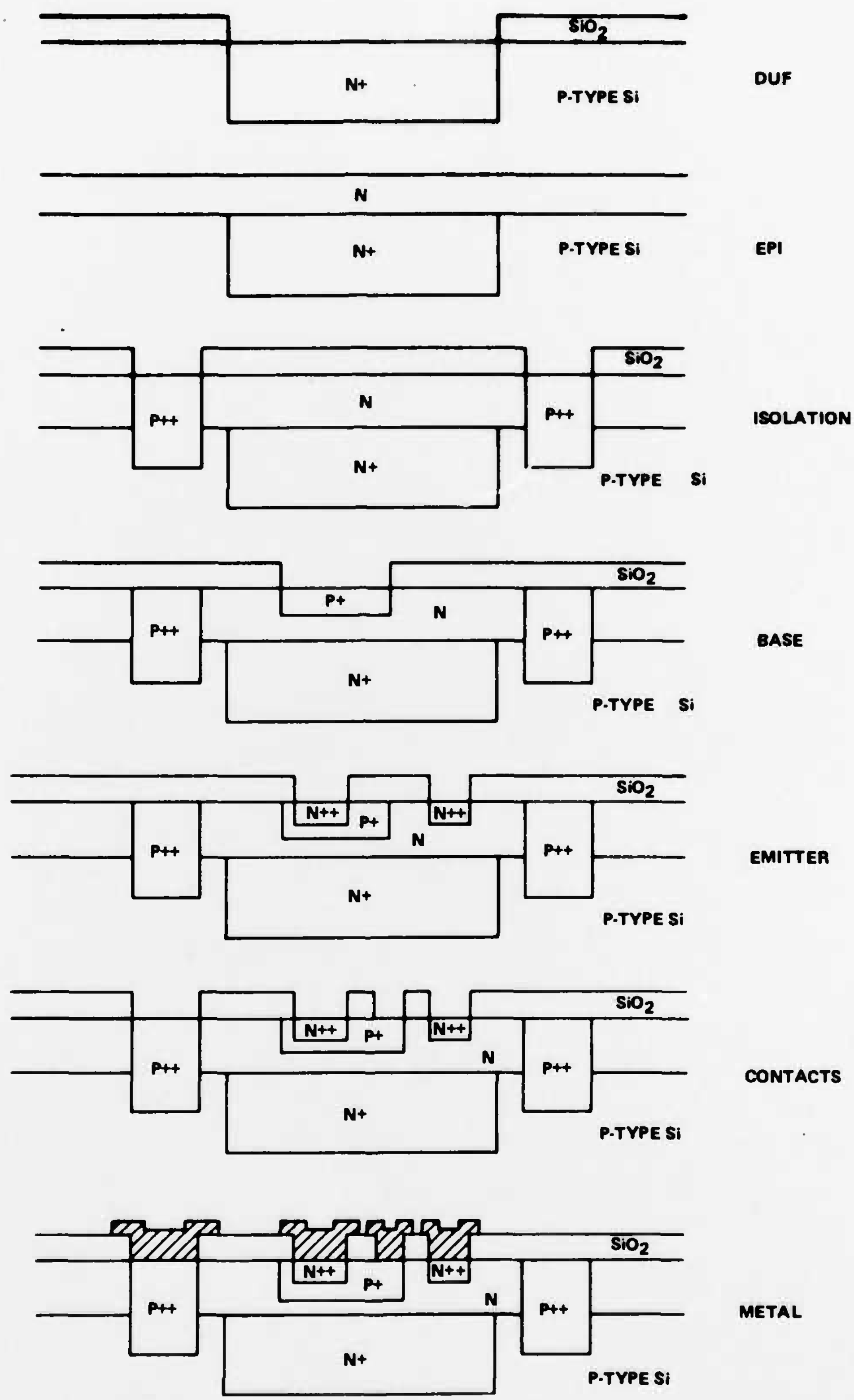


Figure 6. Sectional View of Slice at Various Steps

SECTION III
MANPOWER

The following professionals worked on this program 1 December 1977 to 1 March 1978. The percentage of time worked is also shown.

Mr. P. L. Whelan	20%
Mr. R. A. Williamson	50%
Dr. G. L. Varnell	10%
Dr. J. L. Bartelt	50%
Dr. R. A. Owens	50%
Dr. J. Reynolds	50%
Dr. R. A. Robbins	Consultant
Mr. C. D. Winborn	Consultant

In addition, three technicians worked on the program.

Figure 3. DUF Level (74S301A)

Figure 5. 256-Bit Bipolar RAM-DUF Level – 9000Å Oxide